Analog Integrated Circuits Design (2024-25)

- MOST Operation, Modelling
  - 13-17 Sep MOSFETs: Operation and Modelling
  - 20-24 Sep Noise1 : (in time and frequency domains)
  - 27 Sep-1 Oct Noise-2 : (Analog circuits noise analysis)
- Voltage references and regulators
  - 04 Oct Current Sources and Mirrors
  - 08 Oct Voltage and Temperature independent References
  - 11 Oct Exercises
- OTA and Op-Amp Design
  - **15 Oct** OTA Analysis and Design (DC, AC, Stability …) (1)
  - **18-22-25 Oct Vacation**
  - **29 Oct** OTA Analysis and Design (DC, AC, Stability …) (2)
  - **1 Nov Lab1-a: OTA Structural Design (g_m/I_D Methodology) theory**
  - **05 Nov Lab1-b: OTA Structural Design (g_m/I_D Methodology) Lab (CO5)**
  - 08 Nov: Multistage OTA (Stability and Frequency Compensation)
  - 12 Nov: Fully-Diff Amplifiers & CMFB
  - 15 Nov: Variability, offset and noise in OpAmp (1)
  - **19 Nov Lab2: Fully diff dolded cascode amplifier & its CMFB (CO5)**
  - 22 Nov: Variability, offset and noise in OpAmp (2)
  - 26 Nov: Rail to Rail input and output amplifiers
- Mixed-signal design
  - 29 Nov: Comparators
  - **03 Dec Lab3: Comparators (CO5)**
  - 06-10 Dec: AD and DA converters (introduction)
  - 13 Dec: Digital calibration of analog circuits
- 20 Dec General revision (zoom)

Variability, offset and noise in OpAmp

A. KOUKAB
Swiss Federal Institute of Technology (EPFL)

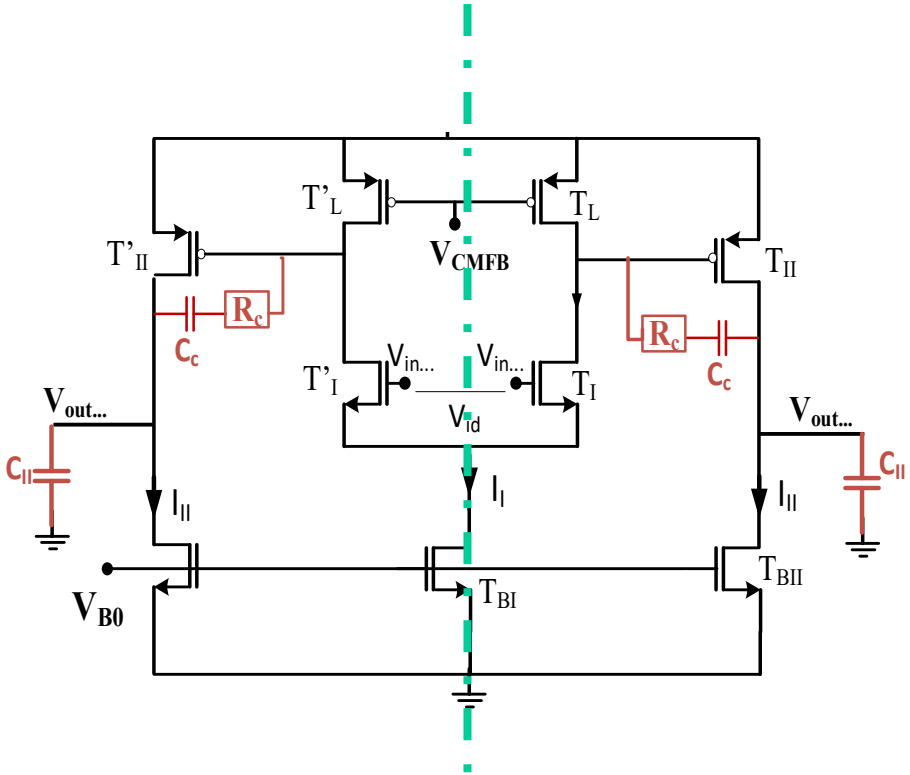
EPFL

Outline

- Variability and Mismatch in CMOS technology
  - Global vs Local Process variations
  - Statistical Analysis (Standard deviation)
  - Design techniques for better matching
  - Layout techniques for better matching
- DC-offset
  - Random offset
  - Systematic offset
  - Impacts on analog and mixed-signal design
- Noise
  - Background
  - Noise in OTA (simple and advanced topologies)
  - Basic methodology for low noise

Process Variation and Mismatch

- Studies of amplifiers usually assume the circuits are perfectly symmetric
- In reality nominally-identical devices suffer from a finite mismatch



- Variation in process parameters
  - Oxide thickness
  - Doping Profile of the channel
  - Channel length/width
  - Silicon/oxide interface traps and charges
  - …
- Variation in electrical parameters
  - Threshold voltage mismatch ΔV_{th}
  - Current factor mismatch $\Delta\beta$

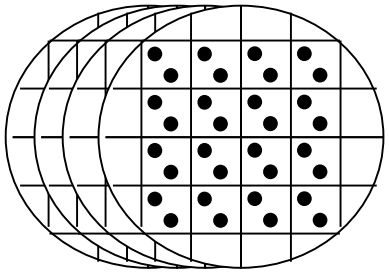
→ Impact the performances

Global vs Local Process variations

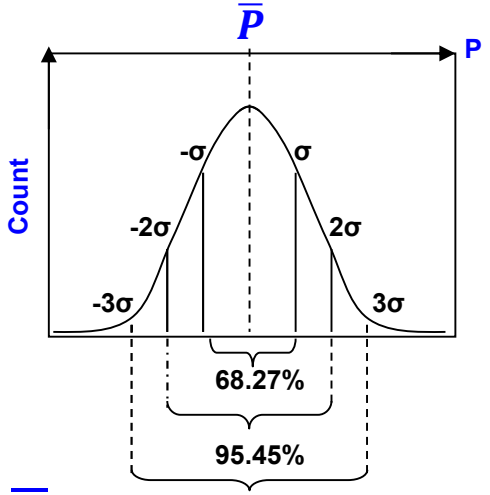
- Two categories of process variations Global and Local:
- Global Process variation or Corners:
  - Represent the parameter variations from wafer-to-wafer and lot-to-lot.
  - Five corners: (TT/FF/SS/FS/SF): F, S, T means Fast, Slow, Typical
  - The first letter refers to nMOS, and the second to pMOS.
  - Independent on the design and layout.
  - More important in digital design
- Local Process Variation or Mismatch
  - Represent the parameter variations from device to device on the same circuit.
  - Dependent on the design and layout.
  - More important in analog design (diff pair, mirrors …)
  - Characterized by a statistical model (standard deviation σ).

Local Process Variation and Mismatch LPVM:

Statistical Analysis (Standard deviation)



Measure Param. (ex V_{th})



- 99.73% of the devices have their P ∈ [$\overline{P}$ -3σ , $\overline{P}$ + 3σ]
- Larger components exhibit smaller mismatches

$$\sigma = A / \sqrt{WL}$$

foundry

$$\frac{\sigma_\beta}{\beta} = \frac{\sigma_{kp}}{kp} = \frac{A_\beta}{\sqrt{WL}} \quad \text{and} \quad \sigma_{V_{T0}} = \frac{A_T}{\sqrt{WL}}$$

Characteristics of σ

$$\sigma_{F(X,Y)}^2 = \sigma_X^2 \left(\frac{\partial F}{\partial X}\right)^2 + \sigma_Y^2 \left(\frac{\partial F}{\partial Y}\right)^2 \; ; \quad \sigma_{G(X,Y)}^2 = \sigma_{F(X,Y)}^2 \left(\frac{dG}{dF}\right)^2$$

Mismatch calculation of I_D and V_G and their optimization by design

- A simple mismatch Model for I_D and V_G (in SI and Sat):
  - based on the assumption that V_T and β are independent

$$I_D = \frac{\beta}{2}(V_G - V_T)^2 \; ; \qquad V_G = \sqrt{\frac{2I_D}{\beta}} + V_T \quad \text{and} \quad \frac{g_m}{I_D} = \frac{2}{V_G - V_T}$$

➢ $\frac{\sigma_{I_D}}{I_D} = ?$

$$\sigma_{I_D(\beta,V_{T0})}{}^2 = \sigma_\beta{}^2 \left(\frac{\partial I_D}{\partial \beta}\right)^2 + \sigma_{V_{T0}}{}^2 \left(\frac{\partial I_D}{\partial V_{T0}}\right)^2$$

$$\left(\frac{\sigma_{I_D}}{I_D}\right)^2 = \left(\frac{\sigma_\beta}{\beta}\right)^2 + \sigma_{V_{T0}}{}^2 \left[\frac{2}{V_G - V_{T0}}\right]^2 = \left(\frac{\sigma_\beta}{\beta}\right)^2 + \sigma_{V_{T0}}{}^2 \left[\frac{g_m}{I_D}\right]^2$$

To minimize ΔI_D → we have to minimize g_m / I_D → Strong Inv.

➢ $\sigma_{V_G} = ?$

$$\sigma_{V_G(\beta,V_{T0})}{}^2 = (\sigma_{I_D})^2 \left(\frac{dV_G}{dI_D}\right)^2 = \left(\frac{\sigma_{I_D}}{g_m}\right)^2 = \left[\frac{I_D}{g_m}\right]^2 \left(\frac{\sigma_\beta}{\beta}\right)^2 + \sigma_{V_{T0}}{}^2 = \left[\frac{I_D}{g_m}\right]^2 \left(\frac{\sigma_{I_D}}{I_D}\right)^2$$

To minimize ΔV_G → we have to maximize g_m / I_D → weak inv.

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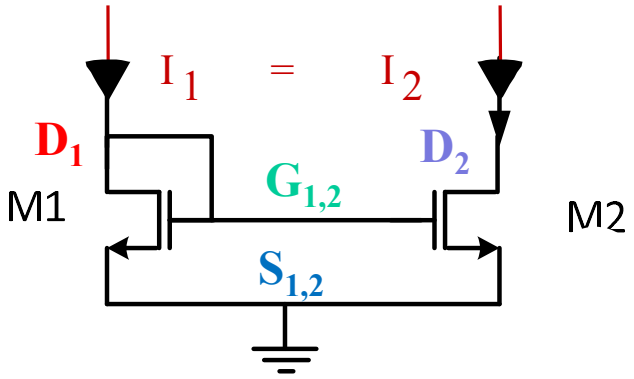
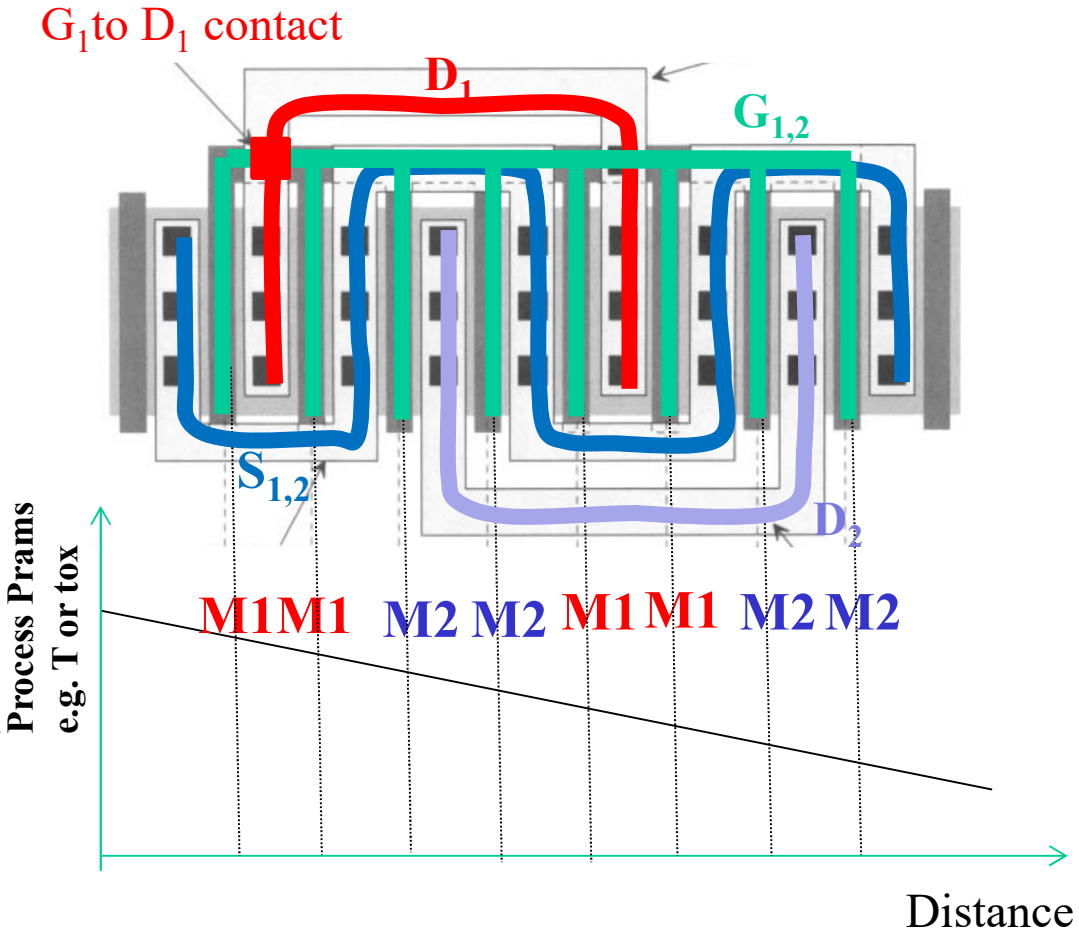
Layout technics for a better matching



Interdigitated and Common centroid Layout



Objective:

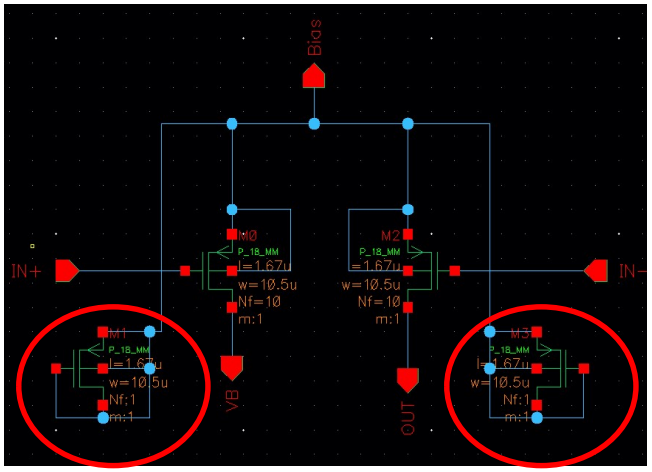
On average, the two devices occupy the same location on the wafer

→ to distribute evenly the influences of process parameters or temperature gradients

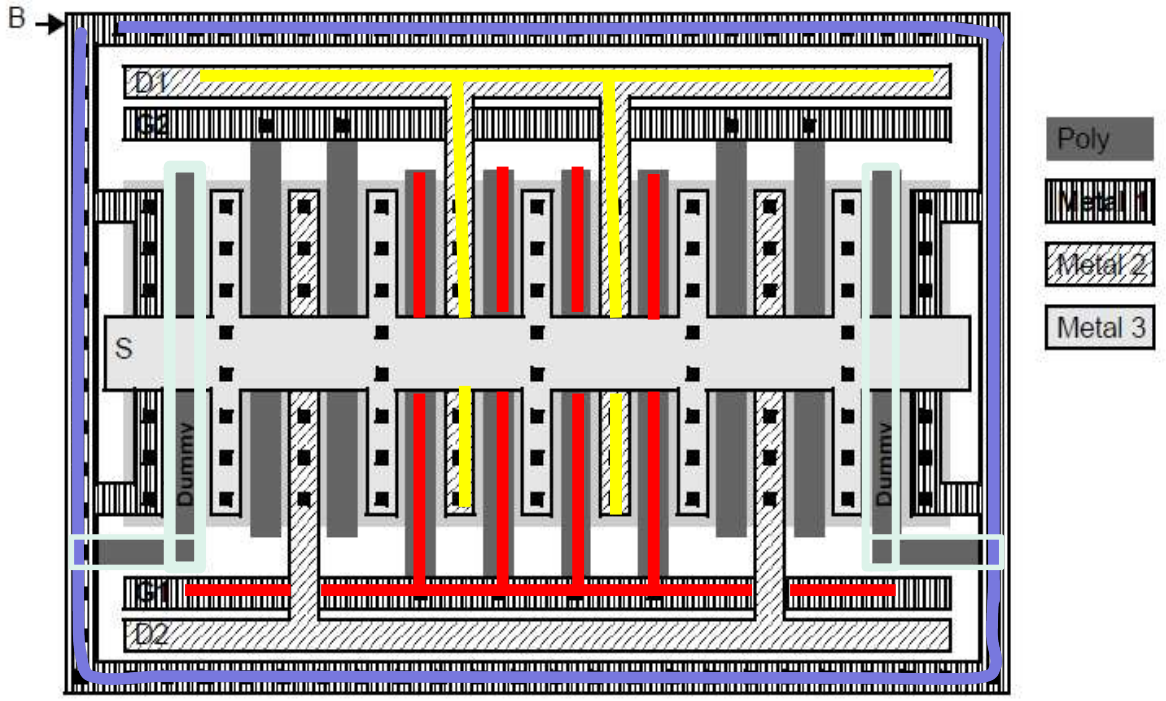
→ to minimize electrical parameters mismatch e.g. V_T and β.

More sophisticated Layout

Guard ring: a ring of contacts encircles the two transistors, providing a low and the same resistance of the body terminals to the ground or V_{DD} → To avoid problems such as latch-up and substrate coupling.



Dif. Pair

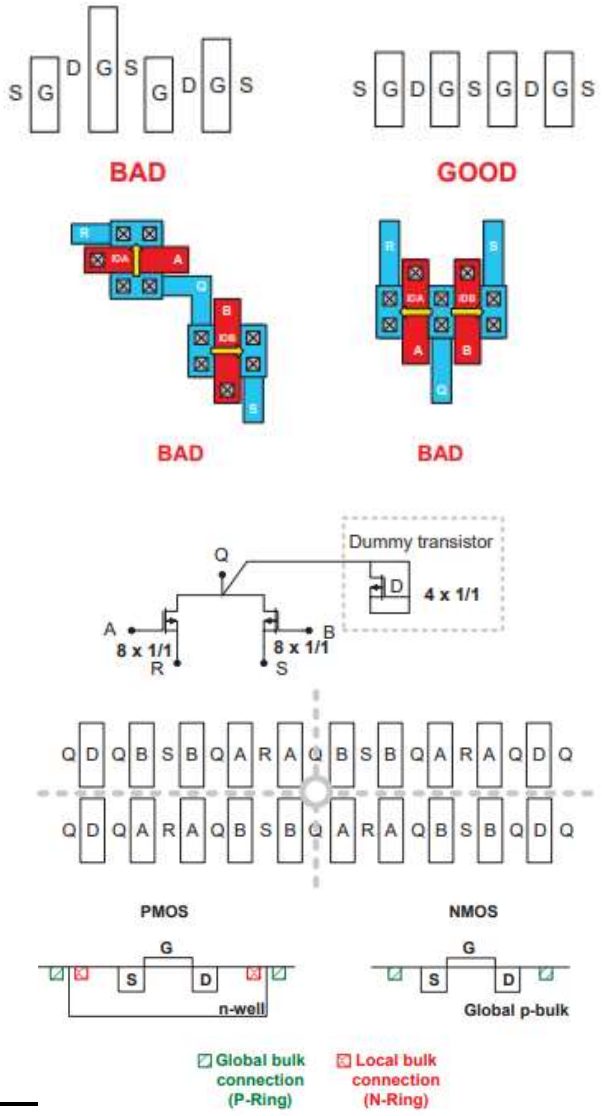


Dummy fingers at the borders → to keep the same environment for each transistor. Their gates are connected to ground (resp. to Vdd) to ensure they are always turned off

Min C_{GD}: Drain connections are routed in the side opposite the gate routing, to minimize parasitic gate-drain (Miller) capacitance.

Layout rules for better matching

- Combine single-sized units to draw transistors (same L same W)
- Keep the layout of the matched transistors as compact as possible
- Orient transistors in the same direction (keep current propagation symmetrical)
- Use interdigitated fingers and common-centroid layout
- Add dummy fingers (in the borders)
- Add a ring of contacts (guard ring) encircling the transistors.
- Use several contacts to connect two different layers in order to reduce interlayer resistance (via are quite resistive)
- Do not place contacts on top of active gate areas (Whenever possible, extend the poly beyond the diffusion and place the gate contacts over thick field oxide.
- Connect gate fingers using metal straps (avoid poly connections. Poly is a bad conductor).
- Do not route metal across the active gate area.



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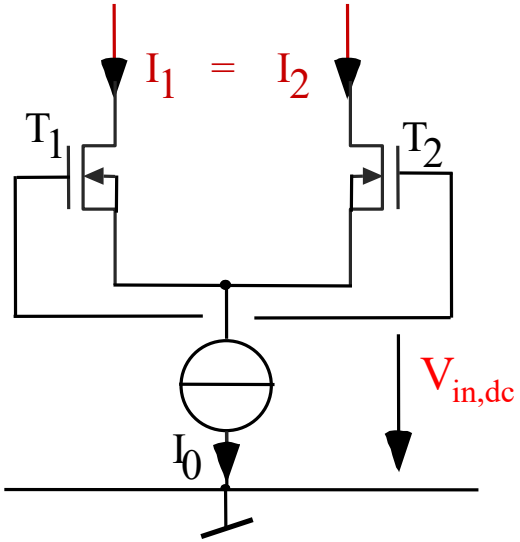
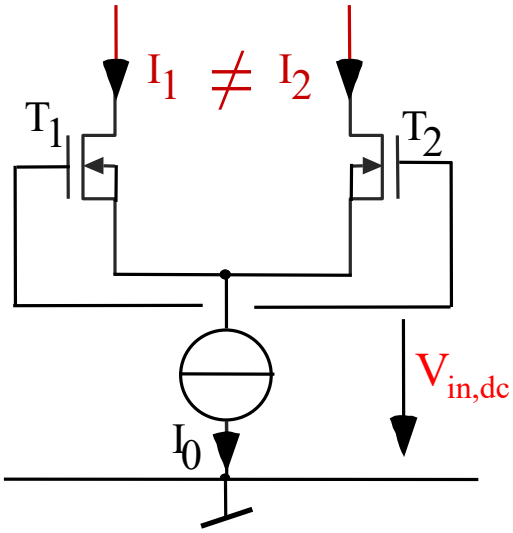
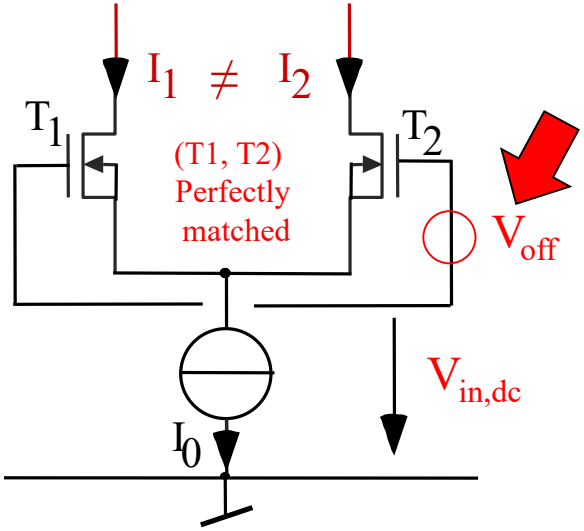
Random DC-offset: (diff. pair)



Ideal diff. pair



Real diff. pair
Radom Mismatch effect
σ_{cox}, σ_{μ} , …



I_D Mismatch
to V_G mismatch
→ V_{off}

$$\sigma_{V_{off}(\beta,V_{T0})}^{2} = \left(\frac{1}{g_m}\right)^2 \sigma_{I_D}^{2}$$

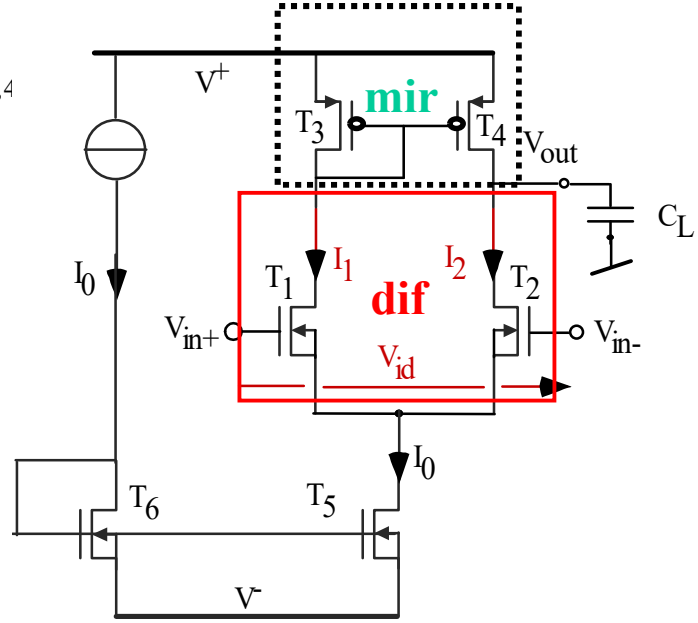
OTA – Random Offset Voltage(V_{off})

with $\frac{\sigma_\beta}{\beta} = \frac{A_\beta}{\sqrt{WL}}, \sigma_{V_{T0}} = \frac{A_T}{\sqrt{WL}}, \quad g_{m,diff} = g_{m1,2}, \quad g_{m,mir} = g_{m3,4}$

$$\sigma_{V_{off}(\beta,V_T)}^2 = \left(\frac{\sigma_{I_{D,dif}}}{g_{m.dif}}\right)^2 + \left(\frac{\sigma_{I_{D,mir}}}{g_{m.dif}}\right)^2$$

$$= \left[\frac{I_0}{2g_{m.dif}}\right]^2 \left(\frac{A_\beta^2}{W_{dif}L_{dif}} + \frac{A_T^2}{W_{dif}L_{dif}} + \right.$$

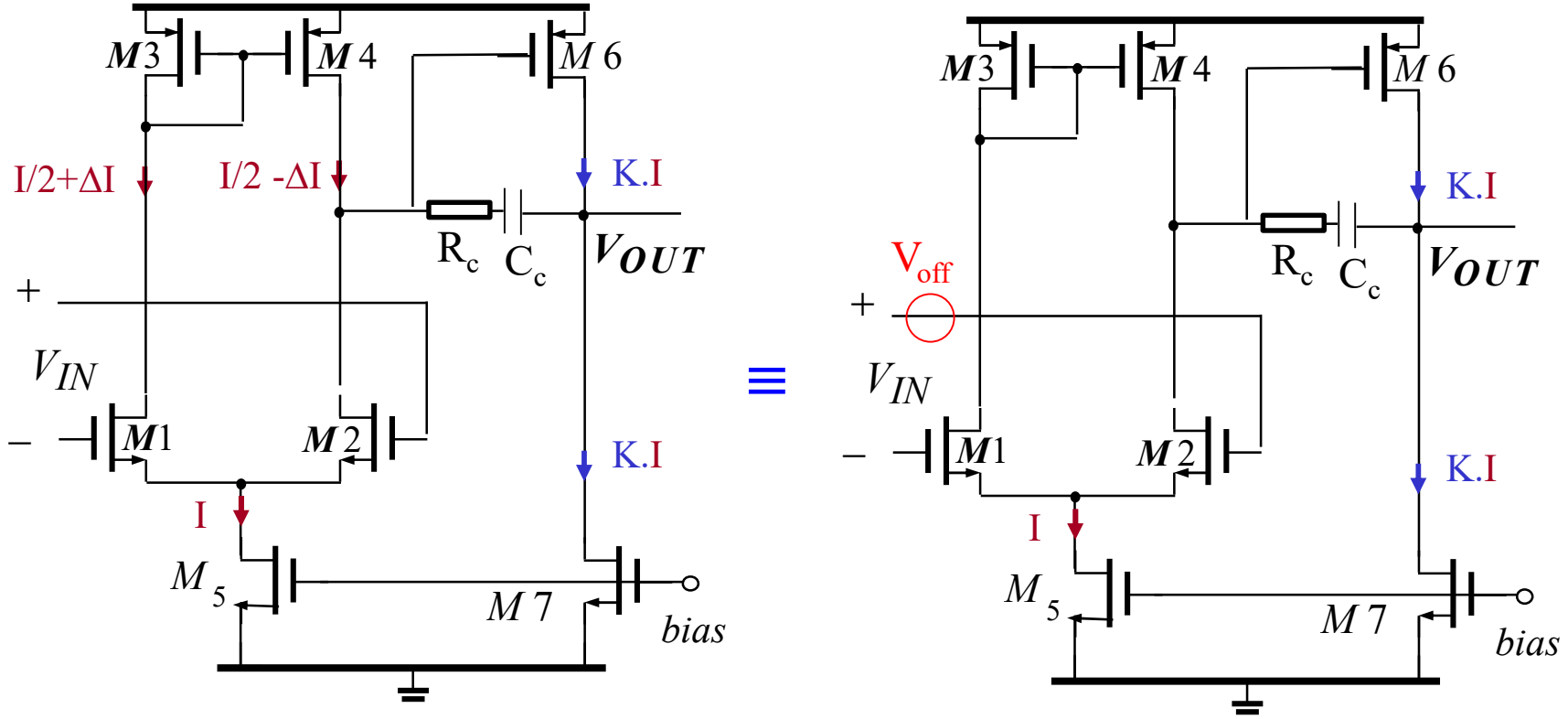
$$\left[\frac{I_0}{2g_{m.dif}}\right]^2 \left(\frac{A_\beta^2}{W_{mir}L_{mir}} + \frac{A_T^2}{W_{mir}L_{mir}} \left(\frac{2g_{m.mir}}{I_0}\right)^2\right)$$



min Offset → Maximize $g_{m,dif}/I_D$ and minimize $g_{m,mir}/I_D$
→ $g_{m,dif} >> g_{m,mir}$
i.e. Diff pair in weak inversion and Active load in strong inversion

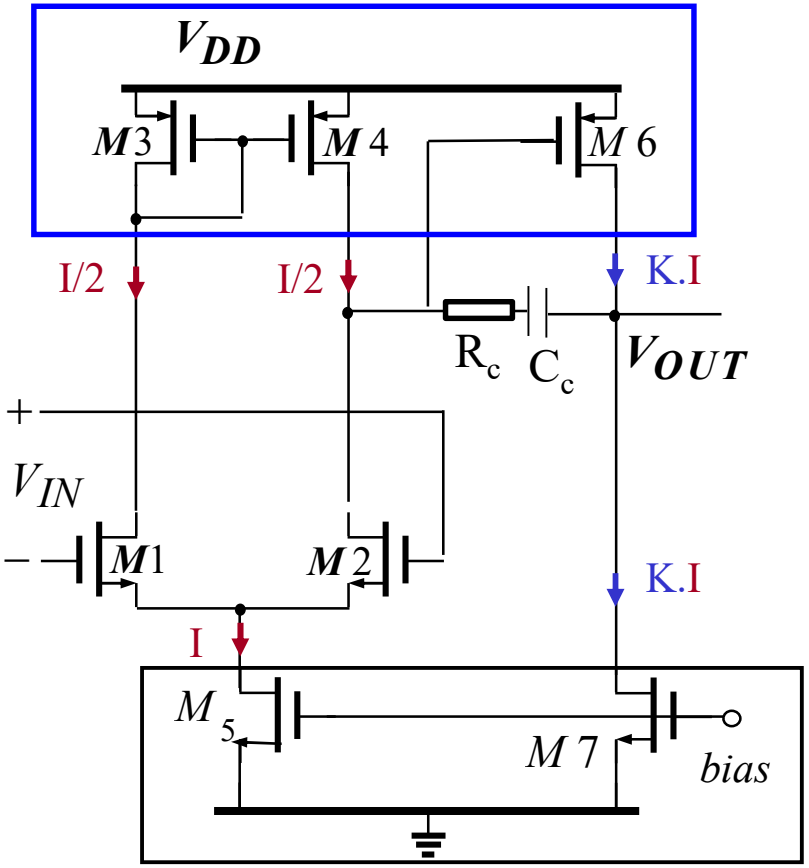
Systematic or Electrical DC-offset:
(Ex. Miller Amp)

- Offset due to asymmetries in the circuits.
- For instance, here, M3 is diode-connected but not M4.
- In addition V_{SD4} is set by M6 ($V_{SD4} = V_{GS6}$)



Systematic DC-offset: Design solution

- M_4, M_3 and M_6 are carefully matched



$$\left(W/L\right)_{M7} = K\left(W/L\right)_{M5}$$

- **Condition for a low systematic offset :**
- **$I_{D3} \approx I_{D4} \approx I/2$ → $V_{SD4} \approx V_{SD3} \approx V_{SG3}$**

Since $V_{SD4} = V_{SG6}$

→ we should have $V_{SG6} \approx V_{SG3}$

$$\left(W/L\right)_{M6} = 2K\left(W/L\right)_{M4,3}$$

- **Residual systematic offset at the input :**

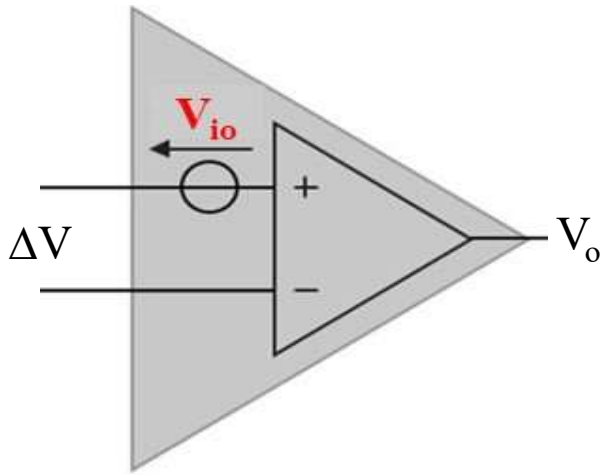
$V_{os,sys} = (V_{D3} - V_{D4})/A_{v1}$

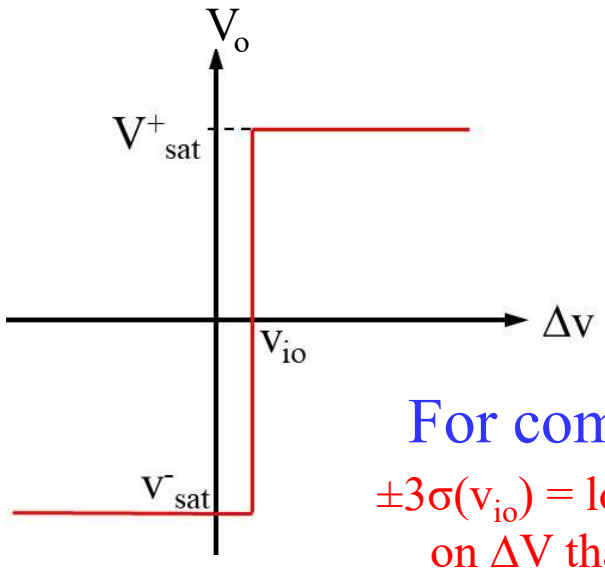
With $A_{v1} = g_{m1}/(g_{DS1} + g_{DS4})$

Offset in Comparators

- Nominally-identical devices of OTA suffer from a finite mismatch
  → represented by an input-referred DC offset voltage

Model of real OTA



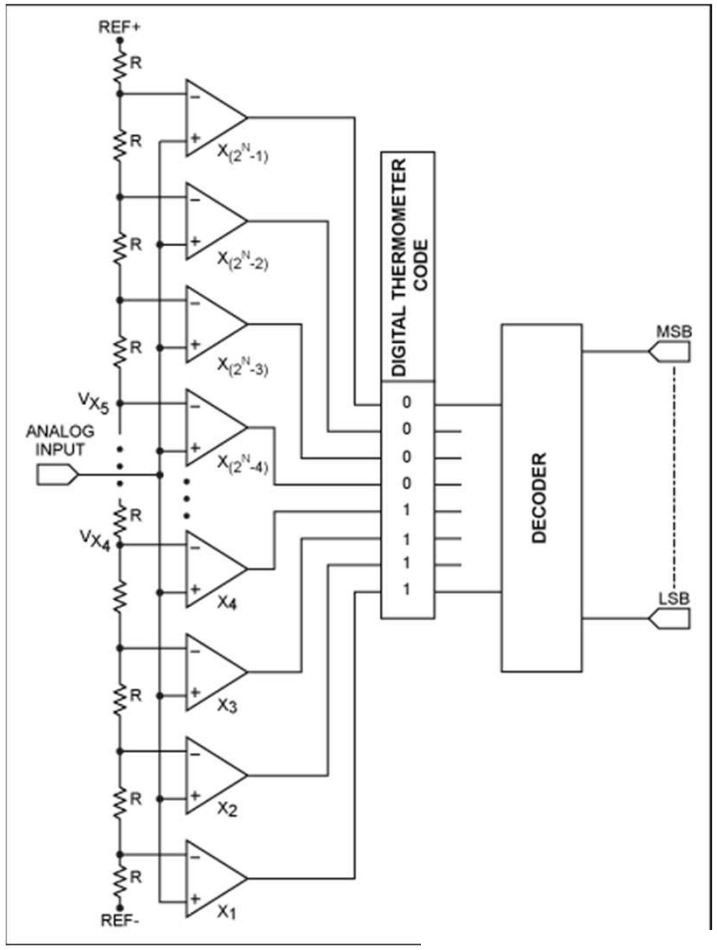


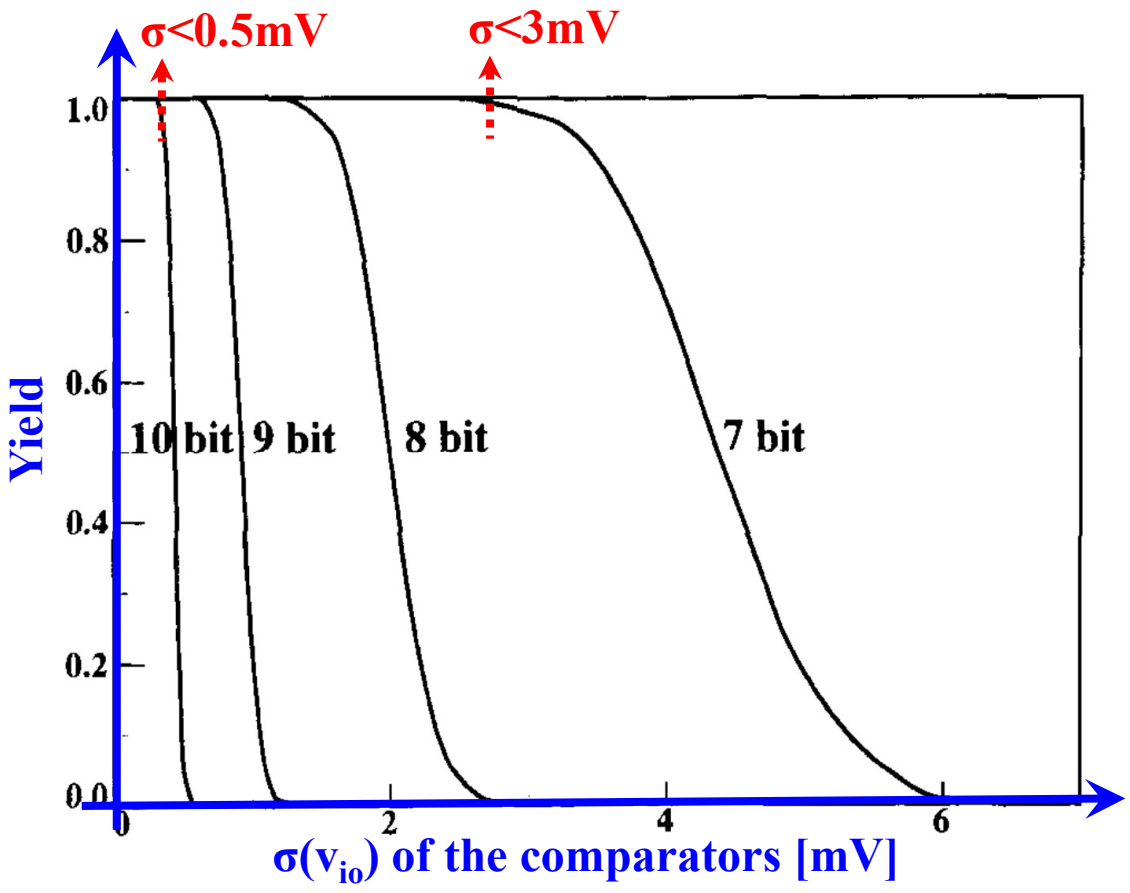
For comparators

$\pm 3\sigma(v_{io})$ = lower bound on ΔV that can be detected reliably

- **Several Offset cancellation Technics exist:**
- **It is worth noting that these technics usually also reduce LF noise and drift**

Lack of accuracy in CMOS comparators: Consequences in ADC Performance





Theoretical Yield on monotonicity (i.e. The probability that the comparators switch in the correct order), here for a signal swing is 2 V

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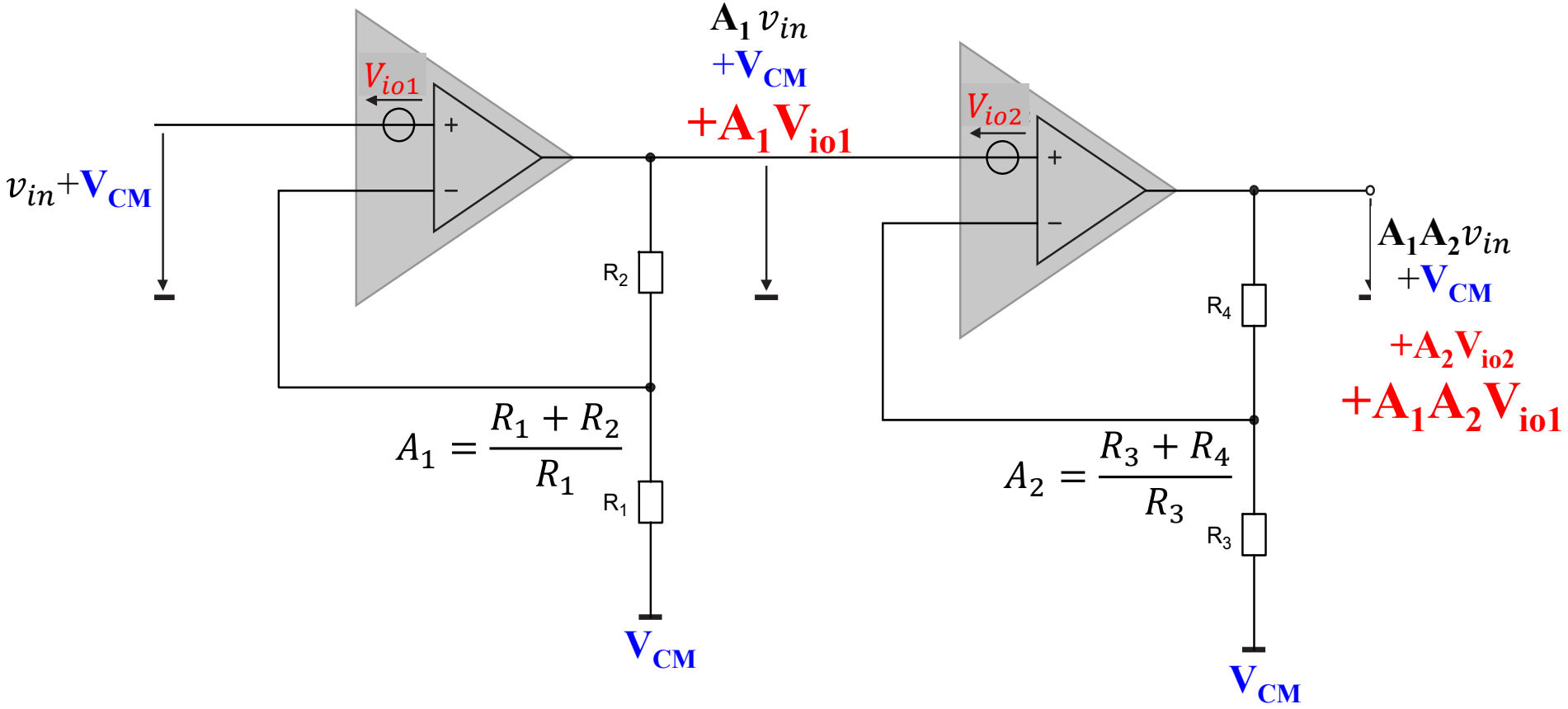
Ref: Yield of n-bit flash ADC Ref. P. Pelgrom & al IEDM 1998

Consequences on dynamic range of amplifiers



DC Offset (meanly V_{io1}) may experience so much gain that it drives the latter stages into nonlinear operation.

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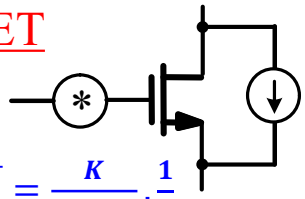
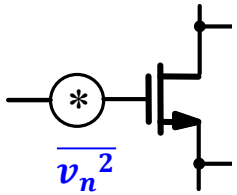
Background 1

MOSFET



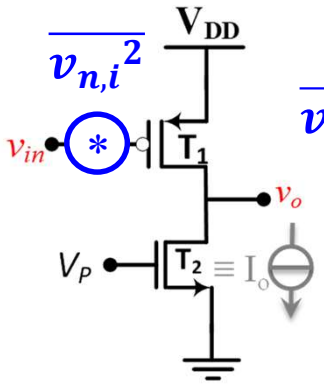
$\overline{i_n^2} = 4kT\gamma g_m$
(Thermal noise)

$\overline{v_n^2} = \frac{K}{C_{ox}LW} \cdot \frac{1}{f}$
(Flicker noise)



$\overline{v_n^2}$
$= 4kT\gamma \frac{1}{g_m} + \frac{K}{C_{ox}LW} \cdot \frac{1}{f}$
(Thermal noise +Flicker noise)

Common source Amp

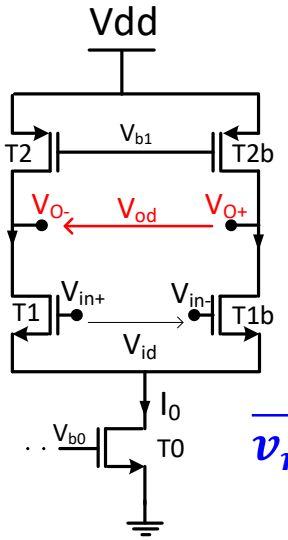


$$\overline{v_{n,i}^2} = \frac{\overline{v_{n,o}^2}}{|A_v|^2} = 4kT\gamma \frac{1}{g_{m1}}\left(1 + \frac{g_{m2}}{g_{m1}}\right) + \frac{K}{C_{ox}(LW)_1} \cdot \frac{1}{f} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \frac{K}{C_{ox}(LW)_2} \cdot \frac{1}{f} \quad [V^2/\,Hz]$$

$\overline{v_{n,i}^2} \searrow$ if $g_{m1} \nearrow$ and $g_{m2} \searrow$

Background 2

Diff Amp

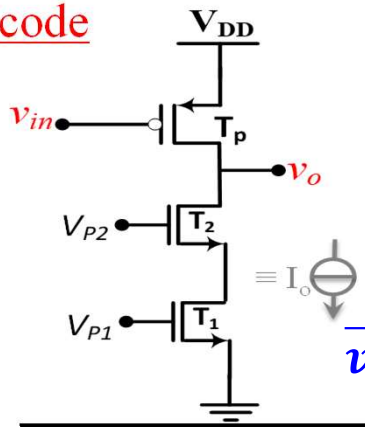


$$\overline{v_{n,i}^2} = 2 \times \left[4kT\gamma \frac{1}{g_{m1}} \left(1 + \frac{g_{m2}}{g_{m1}}\right) + \frac{K}{C_{ox}(LW)_1} \cdot \frac{1}{f} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \frac{K}{C_{ox}(LW)_2} \cdot \frac{1}{f} \right]$$

$Half\ circuit \equiv CS\ amp$

$\overline{v_{n,i}^2}\big|_{T_0}$ negligible (common mode rejection)

Cascode

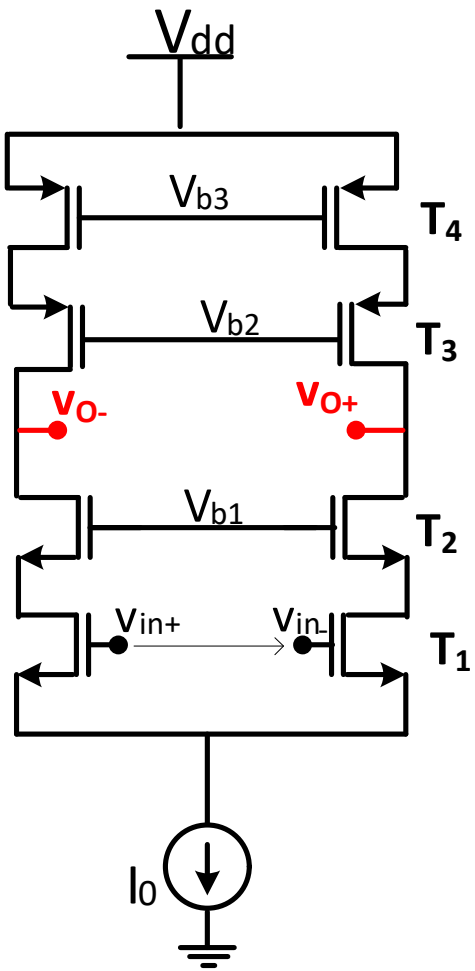


$\overline{v_{n,o}^2}\big|_{T_2}$ negligible (degenerated CS: $\frac{v_o}{v_{pe}} \approx \frac{g_{m2}r_{op}}{1+g_{m2}r_{o1}} \approx \frac{r_{op}}{r_{o1}}$ close to1)

$$\overline{v_{n,o}^2}\big|_{T_1} = \left(4kT\gamma \frac{1}{g_{m1}} + \frac{K}{C_{ox}(LW)_1} \cdot \frac{1}{f}\right) \left(g_{m1}\left(r_{op} \| g_{m2}(r_{on1} r_{on2})\right)\right)^2$$

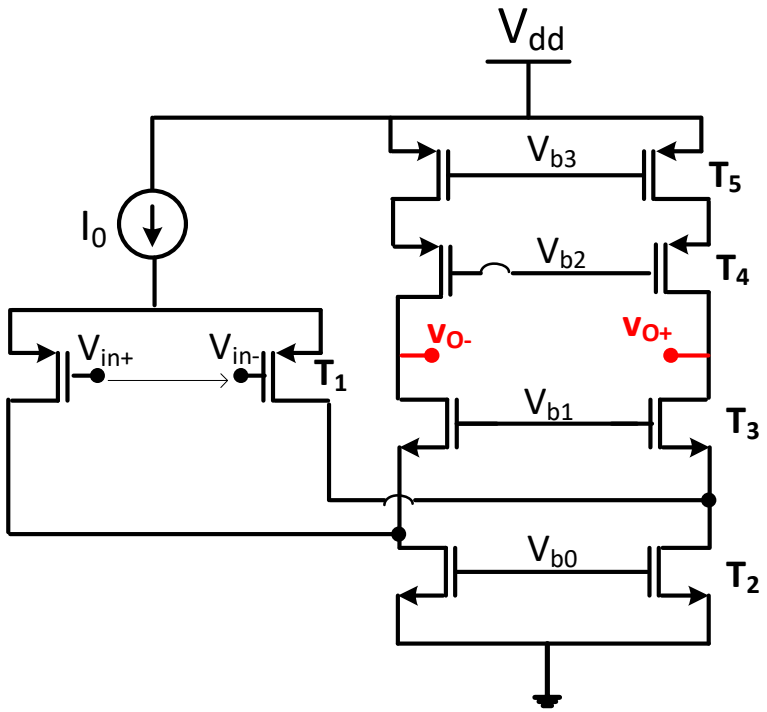
$>> 1$

Noise in Telescopic Amp.



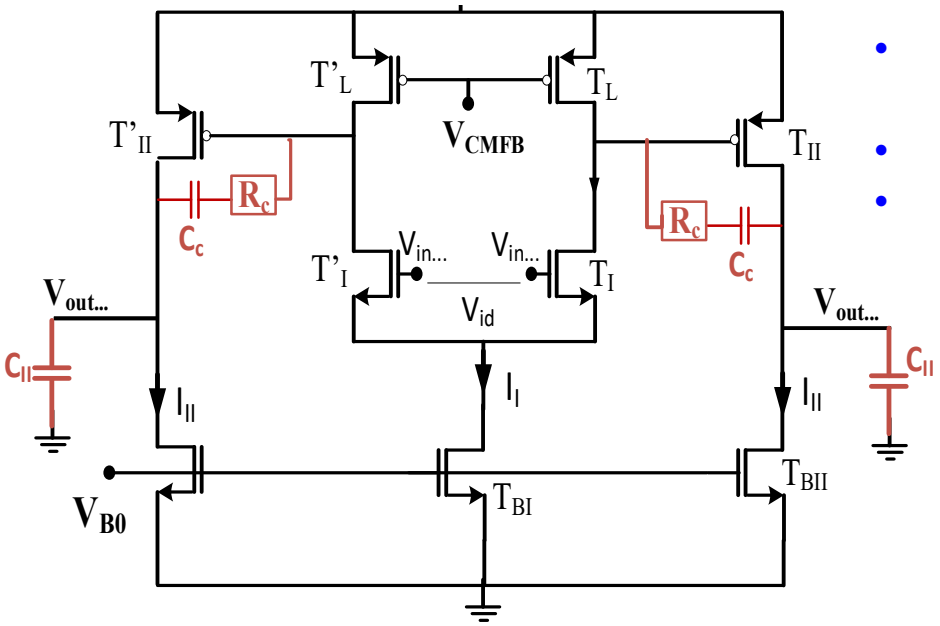
- Give the main noise contributors
- Determine the input-referred noise $\overline{v_{n,i}^2}$
- Propose I_F (or V_{ov}) of the transistors to optimize the noise
- Discuss the resulted tradeoffs (noise vs offset, dynamic range and consumption)
- Prose a solution to optimize flicker noise

Noise in Folded cascode amp.



- Give the main noise contributors and compare with Telescopic
- Determine the input-referred noise $\overline{v_{n,i}^2}$
- Propose I_F (or V_{ov}) of the transistors to optimize the noise
- Discuss the resulted tradeoffs (noise vs offset, dynamic range and consumption)

Noise in Miler amp.



- Give the main noise contributors
- Determine the input-referred noise $\overline{v_{n,i}^2}$
- Propose I_F (or V_{ov}) of the transistors to optimize the noise
- Comment on Vov of T_L
- Compare with the other topologies